Abstract

[0053] An improved high performance scheme is provided with a serial peripheral interface (SPI) to enable microcontroller-based products and other components and devices to achieve a higher serial transmit and receive data rate. An exemplary technique utilizes a CPU and an SPI having a circular FIFO structure. To prevent the memory traffic associated with any SPI accesses from conflicting with other CPU memory accesses, the technique utilizes cycle stealing direct memory access techniques for SPI data transfers with the memory. During a CPU read/write sequence, data is read/written from/to the memory through a virtual special function register (SFR). Once the virtual SFR access is detected, all accesses are redirected to the circular FIFO buffer memory, with no additional pipelining necessary. The CPU pointers can suitably increment as appropriately controlled by hardware. In addition, once an SPI transmit/receive request is made, data communication can be established between the transmit/receive buffer and the memory. To avoid structural hazard, the transmit/receive request can be suitably pipelined until the next available clock phase, for example, within one instruction cycle. As a result, for a 4 Mhz clock rate, the technique can enable a significantly higher data transfer rate, *e.g.*, at 250 Kbytes per second, an improvement of almost twenty times the prior art data rates. The high performance technique also avoids the firmware overhead with minimum hardware control cost. For example, compared to the hardware approach using deeper buffer structures, *e.g.*, with FIFO buffers implemented using flip-flop devices, the exemplary techniques utilize memory, *e.g.*, dynamic or static random access memory (DRAM or SRAM) with direct memory access (DMA).